AMENDMENTS TO THE SPECIFICATION

Please amend the title of the application on page 1 and page 10 of the specification as follows:

An Electric Device Having ~~A Method for Making~~ Nanoscale Wires and Gaps ~~for Switches and Transistors~~

Please amend the first sentence on page 1 of the specification (as amended) as follows:

This application is a divisional of prior Application No: 10/104,438 filed March 22, 2002, now U.S. Patent No. 6,699,779.

Please amend the paragraph on page 5, lines 8-20, as follows:

Refer now to Figure 3, which is a perspective view of a silicon nanowire structure that forms a switch or a transistor. Transistor 30 is constructed from two silicon nanowires shown at 32 and 33. Nanowire 33 acts as the gate of transistor 30. The ends of nanowire 32 form the source and drain of transistor 30. Nanowires 32 and 33 are fabricated using a mask of the type shown in Figure 1B [[2]]. Due to the small gap distance 34, when a voltage is applied on nanowire 32, the electric field will influence and control the current flow in nanowire 33. The gap can be filled with a material such as molecules, ferroelectric materials, and nanoscale particles that store charge or electric dipole moment in the gap. Hence, the transistor can provide gain or nonvolatile switching for logic and memory applications. If two-electrode devices are formed between the nanowires 32 and 33, an electric field applied between the two electrodes can switch the electric conductivity of the materials adjacent to the gap. Such a device is taught in US Patent 6,128,214, which describes how a memory cell can be formed between the two nanowires.